Notice of Allowability	Application No. 10/701,471	Applicant(s) INOUE, HIROHITO	
	Examiner Roberto Velez	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/30/2007*.

2. ☒ The allowed claim(s) is/are *1-8*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 11/06/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Nils Pedersen on 08/16/2007.

2. The application has been amended as follows:

Claim 1 (Currently Amended) A wafer handling checker comprising: a plurality of training operation wafers each formed of a semiconductor or ceramic[[s]] material to which a conductive film or a material having conductive properties is applied on a face thereof [[, or a material having conductive properties]]; a cassette having a plurality of slots for housing the plurality of training operation wafers, and a plurality of electrodes for contacting the plurality of training operation wafers when the plurality of training operation wafers are inserted into the plurality of slots; a vacuum pincette having a conductive suction part for operating on the plurality of training operation wafers; voltage application means for applying a voltage between each electrode of the cassette and the conductive suction part of the vacuum pincette; and state detection means for detecting which of the plurality of training operation wafers housed in the cassette the vacuum pincette is in contact with by detecting a potential of each

electrode of the cassette or a current flowing to an electrode of the cassette associated with the contacted training operation wafer.

Claim 5 (Currently Amended) A wafer handling checker comprising: a plurality of training operation wafers each formed of a semiconductor or ceramic[[s]] material to which a conductive film or a material having conductive properties is applied on a face thereof [[, or a material having conductive properties]]; a cassette having a plurality of slots for housing the plurality of training operation wafers, and a plurality of electrodes for contacting the plurality of training operation wafers when the plurality of training operation wafers are inserted into the plurality of slots; a vacuum pincette having a conductive suction part for operating on the plurality of training operation wafers; and a controller [[operable]] configured to apply a voltage between each electrode of the cassette and the conductive suction part of the vacuum pincette, and detect which of the plurality of training operation wafers housed in the cassette the vacuum pincette is in contact with by detecting a potential of each electrode of the cassette or a current flowing to an electrode of the cassette associated with the contacted training operation wafer.

Claim 6 (Previously Presented) The wafer handling checker according to Claim 5, wherein the cassette has a display [[operable]] configured to specify a training operation wafer to be operated on based on operation specification information.

Claim 7 (Previously Presented) The wafer handling checker according to Claim 6, wherein the controller is further [[operable]] configured to decide whether an erroneous operation occurs based on a result of detection and the operation specification information.

Claim 8 (Previously Presented) The wafer handling checker according to Claim 7, wherein the controller is further [[operable]] configured to cause a sound to be generated when the erroneous operation has occurred.

Allowable Subject Matter

3. Claims 1-8 are allowed.

The following is a statement of reasons for allowance: the prior art of record, taken alone or in combination, fails to disclose or render obvious, a wafer handling checker comprising: a cassette having a plurality of slots for housing the plurality of training operation wafers, and a plurality of electrodes for contacting the plurality of training operation wafers when the plurality of training operation wafers are inserted into the plurality of slots; a vacuum pincette having a conductive suction part for operating on the plurality of training operation wafers; voltage application means for applying a voltage between each electrode of the cassette and the conductive suction part of the vacuum pincette; and state detection means for detecting which of the plurality of training operation wafers housed in the cassette the vacuum pincette is in contact with by detecting a potential of each electrode of the cassette or a current flowing to an electrode of

the cassette associated with the contacted training operation wafer, as further disclosed in claim 1;

a wafer handling checker comprising: a cassette having a plurality of slots for housing the plurality of training operation wafers, and a plurality of electrodes for contacting the plurality of training operation wafers when the plurality of training operation wafers are inserted into the plurality of slots; a vacuum pincette having a conductive suction part for operating on the plurality of training operation wafers; and a controller configured to apply a voltage between each electrode of the cassette and the conductive suction part of the vacuum pincette, and detect which of the plurality of training operation wafers housed in the cassette the vacuum pincette is in contact with by detecting a potential of each electrode of the cassette or a current flowing to an electrode of the cassette associated with the contacted training operation wafer, as further disclosed in claim 5.

Claims 2-4 and 6-8 depending from claims 1 or 5 are allowed for the same reason.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ohsawa et al. (US Pat. 5,645,391) discloses a substrate transfer apparatus, and method of transferring substrates.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Roberto Velez
Patent Examiner

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER